IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	:	
	:	Examiner:
Anne KASZYNSKI & Jacques ABILY	:	
	::	
Serial No.: To be assigned.	:	Group Art Unit:
	:	
Filed: Concurrently herewith	:	Corresponding to:
	:	French Patent
	:	Application FR 02 09691
For: **Procédé de vérification fonctionnelle d'un modèle de circuit intégré pour constituer une plate-forme de vérification, équipement émulateur et plate-forme de vérification.** English title (when application is translated) Method for Functional Verification of an Integrated Circuit Model in Order to Create a Verification Platform, Equipment Emulator and Verification Platform	:	Dated July 30, 2002

McLean, Virginia

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following amendments and remarks are submitted prior to examination of the above-identified application on the merits.

Amendments to the Claims are reflected in the listing of claims beginning on page 3 of this paper. The application is being filed in the French language. The amendments to the claims comprise only the elimination of the multiple dependent claims in the French text of the application. An English translation of the application and a Supplemental Preliminary Amendment amending the claims in English will be submitted upon response to the Notice to File Missing Parts – Filing Date Granted.

Remarks begin on page 10.